## IN THE SPECIFICATION:

Please amend the paragraph at page 10, lines 4 to 15 as follows:

-- Figs. 3A to 3J are timing charts illustrating the normal read operation with reset, and Figs. 4A to 4J are timing charts illustrating the non-destructive read operation without rest reset. First, with reference to Figs. 3A to 3J, the normal read operation will be described. As shown in Fig. 3A, during the normal read operation, a high level mode switching signal is supplied from the comparator 112 to the AND gate 132. In this state, as shown in Fig. 3B, when a signal φO<sub>n</sub> (high level) is output from the vertical shift register 130, the vertical output switching MOS transistor 137 is turned on. --